ENA Engineering Recommendation G83

Issue 2 2012

Type Verification Test Report

Type Approval and manufacturer/supplier declaration of compliance with the requirements of Engineering Recommendation G83/2.			
SSEG Type reference number			
SSEG Type	GW3648D-ES / GW3648S-ES		
System Supplier name	Jiangsu GoodWe Power Supply Technology Co.,Ltd.		
Address	NO.189 Kun Lun Shan Road, Suzhou New District, Jiangsu,china		
Tel	+86 512 6239 7998	**Fax**	+86 512 6239 7972
E:mail	service@goodwe.com.cn	**Web site**	http://www.goodwe.com.cn
Maximum rated capacity(use separate sheet if more than one connection option)	**Connection Option**		
	3.6	**kW single phase**	

SSEG manufacturer/supplier declaration.
I certify on behalf of the company named above as a manufacturer/supplier of Small Scale Embedded Generators, that all products manufactured/supplied by the company with the above SSEG Type reference number will be manufactured and tested to ensure that they perform as stated in this Type Verification Test Report, prior to shipment to site and that no site modifications are required to ensure that the product meets all the requirements of G83/2.

Signed	Xie Jing	**On behalf of**	Huang min

Power Quality. Harmonics The requirement is specified in section 5.4.1, test procedure in Annex A or B 1.4.1						**P**
SSEG rating per phase (rpp)					NV=MV*3.68/rpp	
	At 45-55% of rated ouput kW		100% of rated output kW			
Harmonic	Measured Value (MV) in Amps	Normalised Value (NV) in Amps	Measured Value (MV) in Amps	Normalised Value (NV) in Amps	Limit in BS EN61000-3-2 in Amps	Higher limit for odd harmonics 21 and above
2nd	0.024	0.019	0.021	0.017	1.080	
3rd	0.014	0.011	0.032	0.026	2.300	
4th	0.002	0.001	0.007	0.006	0.430	
5th	0.017	0.014	0.025	0.020	1.140	
6th	0.003	0.003	0.005	0.004	0.300	
7th	0.015	0.012	0.032	0.025	0.770	
8th	0.001	0.001	0.007	0.005	0.230	
9th	0.012	0.010	0.032	0.026	0.400	
10th	0.002	0.001	0.008	0.007	0.184	
11th	0.009	0.007	0.031	0.025	0.330	
12th	0.002	0.002	0.008	0.007	0.153	
13th	0.011	0.009	0.028	0.023	0.210	
14th	0.002	0.002	0.010	0.008	0.131	
15th	0.006	0.005	0.024	0.019	0.150	
16th	0.002	0.002	0.010	0.008	0.115	
17th	0.006	0.005	0.021	0.017	0.132	
18th	0.002	0.001	0.013	0.010	0.102	
19th	0.006	0.005	0.020	0.016	0.118	
20th	0.001	0.001	0.011	0.009	0.092	
21th	0.003	0.003	0.018	0.014	0.107	0.160
22th	0.001	0.001	0.010	0.008	0.084	
23th	0.002	0.001	0.014	0.011	0.098	0.147
24th	0.001	0.001	0.011	0.009	0.077	
25th	0.002	0.002	0.015	0.012	0.090	0.135
26th	0.001	0.000	0.010	0.008	0.071	
27th	0.002	0.001	0.013	0.010	0.083	0.124
28th	0.001	0.000	0.010	0.008	0.066	
29th	0.001	0.000	0.009	0.007	0.078	0.117
30th	0.001	0.000	0.007	0.005	0.061	
31th	0.001	0.000	0.007	0.006	0.073	0.109
32th	0.001	0.000	0.005	0.004	0.058	
33th	0.001	0.001	0.006	0.005	0.068	0.102
34th	0.001	0.000	0.005	0.004	0.054	
35th	0.001	0.001	0.008	0.006	0.064	0.096

36th	0.001	0.000	0.006	0.005	0.051	
37th	0.001	0.001	0.008	0.006	0.061	0.091
38th	0.001	0.001	0.008	0.007	0.048	
39th	0.001	0.001	0.010	0.008	0.058	0.087
40th	0.001	0.001	0.008	0.006	0.046	

Note:
The higher limits for odd harmonics 21 and above are only allowable under certain conditions, if these higher limits are utilised please state the exemption used as detailed in part 6.2.3.4 of BS EN 61000-3-2 in the box below.

Flicker
The requirement is specified in section 5.4.2, test procedure in Annex A or B 1.4.3

P

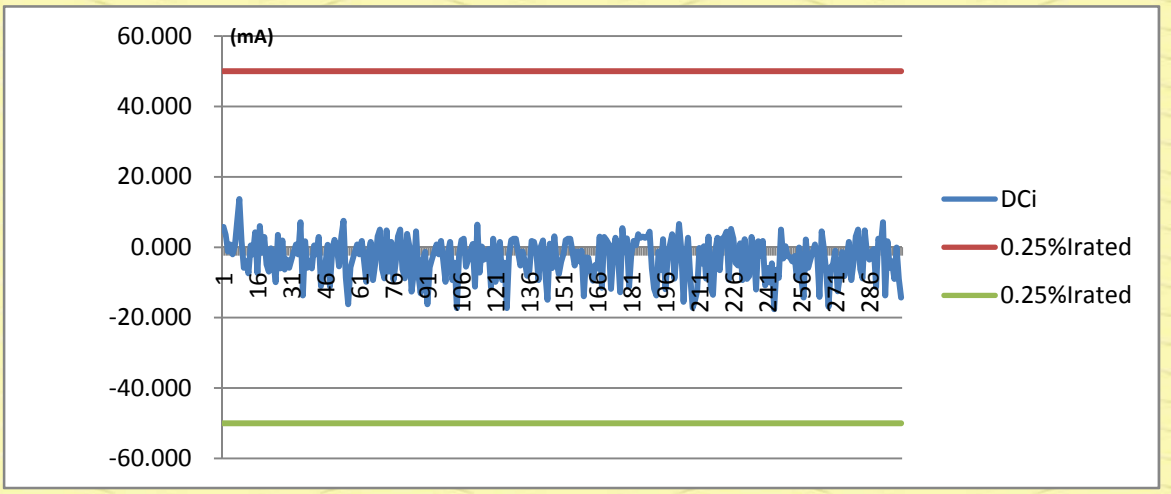
	Starting			Stopping			Running	
	d_{max}	d_c	$d_{(t)}$	d_{max}	d_c	$d_{(t)}$	d_{max}	d_c
Measured values	0	0	0	0	0	0	0	0
Normalised to standard impedance and 3.68kW for multiple units	0	0	0	0	0	0	0	0
Limits set under BS EN 61000-3-2	4%	3.3%	3.3% 500ms	4%	3.3%	3.3% 500ms	4%	3.3%
Test start date	2014/1/10 8:45			Test end date			2014/1/10 10:45	

Power quality. DC injection
The requirement is specified in section 5.5, test procedure in Annex A or B 1.4.4

P

Test level power	10%	55%	100%
Recorded value	8.1 mA	7.5 mA	6.2 mA
As % of rated AC current	0.04%	0.04%	0.03%
Limit	0.25%	0.25%	0.25%

Diagramm of permanent DC-Injec



Power Quality. Power factor The requirement is specified in section 5.6, test procedure in Annex A or B 1.4.2				**P**
	216.2 V	230 V	253 V	Measured at three voltage levels and at full output. Voltage to be maintained within ±1.5% of the stated level during the test.
Measured value	0.998	0.998	0.998	
Limit	>0.95	>0.95	>0.95	

Protection. Frequency test The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.3					**P**	
Function	Setting		Trip test		No trip test	
	Frequency	Time delay	Frequency	Time delay	Frequency / time	Confirm no trip
U/F stage 1	47.5 Hz	20 s	47.53 Hz	19.02 s	47.7Hz / 25s	no trip
U/F stage 2	47 Hz	0.5 s	47.03 Hz	451 ms	47.2Hz / 19.98s	no trip
					46.8Hz / 0.48s	no trip
O/F stage 1	51.5 Hz	90 s	51.47 Hz	85.3 s	51.3Hz / 95s	no trip
O/F stage 2	52 Hz	0.5 s	51.07 Hz	392 ms	51.8Hz / 89.98s	no trip
					52.2Hz / 0.48s	no trip

Protection. Voltage test The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.2					**P**	
Function	Setting		Trip test		No trip test	
	Voltage	Time delay	Voltage	Time delay	Voltage / time	Confirm no trip
U/V stage 1	200.1 V	2.5 s	202.1 V	2.94 s	204.1V / 3.5s	no trip
U/V stage 2	184 V	0.5 s	186 V	930 ms	188V / 2.48s	no trip
					180V / 0.48s	no trip
O/V stage 1	262.2 V	1.0 s	260.1 V	1.42 s	258.2V 2.0s	no trip
O/V stage 2	273.7 V	0.5 s	271.8 V	723 ms	269.7V 0.98s	no trip
					277.7V 0.48s	no trip

Protection. Loss of Mains test inverters can be tested to BS EN 62116.						
Test Power and imbalance	33% -5% Q	66% -5% Q	100% -5% P	33% +5% Q	66% +5% Q	100% +5% P
Trip time. Limit is 0.5s	0.41 s	0.42 s	0.43 s	0.42 s	0.38 s	0.40 s

Protection. Frequency change, Stability test The requirement is specified in section 5.3.3, test procedure in Annex A or B 1.3.6				**P**
	Start Frequency	Change	End Frequency	Confirm no trip
Positive Vector Shift	49.5Hz	+9 degrees		no trip
Negative Vector Shift	50.5Hz	- 9 degrees		no trip
Positive Frequency drift	49.5Hz	+0.19Hz/sec	51.5Hz	no trip
Negative Frequency drift	50.5Hz	-0.19Hz/sec	47.5Hz	no trip

Protection. Re-connection time The requirement is specified in section 5.3.4 Automatic Reconnection, test procedure in Annex A or B 1.3.5	**P**
Test should prove that the reconnection sequence starts after a minimum delay of 20 seconds for restoration of voltage and frequency to within the stage 1 settings of table 1.	
Voltage	
Time delay setting	Measured delay time(s)
20s	43.1 s
Frequency	
Time delay setting	Measured delay time(s)
20s	42.5 s

	Checks on no reconnection when voltage or frequency is brought to just outside stage 1 limits of table 1.			
	At 266.2V	At 196.1V	At 47.4Hz	At 51.6Hz
Confirmation that the SSEG does not re-connect.	no reconnection	no reconnection	no reconnection	no reconnection

Fault level contribution The requirement is specified in section 5.7, test procedure in Annex A or B 1.4.6					**P**
For a directly coupled SSEG			For a Inverter SSEG		
Parameter	Symbol	Value	Time after fault	Volts	Amps
Peak Short Circuit current	-	-	20ms	-13.5 V	350 mA
Initial Value of aperiodic current	-	-	100ms	12.1 V	350 mA
Initial symmetrical short-circuit current*	-	-	250ms	15.5 V	320 mA
Decaying (aperiodic) component of short circuit current*	-	-	500ms	13.5 V	370 mA
Reactance/Resistance Ratio of source*	-	-	Time to trip	560 µs	In seconds

Self Monitoring – Solid state Disconnection The requirement is specified in section 5.3.1, No specified test requirements.	**N/A**
Not applicable since electro-mechanical relays are used.	

Additional comments
GW3648D-ES is similar to GW3648S-ES in circuit and construction except for dual mppt. The test result can refer to GW3648S-ES .